What is claimed is:

1. A semiconductor memory device comprising:

a device substrate having a semiconductor layer separated by a dielectric layer from a base substrate;

a memory cell array having a plurality of memory cells formed and arranged on said semiconductor layer of said device substrate, each said memory cell having a MOS transistor structure with a body in an electrically floating state to store data based on a majority carrier accumulation state of said body; and

a sense amplifier circuit configured to read out data of a selected memory cell in said memory cell array to store the read data in a data latch, then transfer the read data to an output circuit and write back the read data into said selected memory cell.

2. The semiconductor memory device according to claim 1, wherein

the read operation of said sense amplifier circuit is to detect cell current of a selected memory cell by applying gate and drain voltages to turn on it, said drain voltage being set higher than a first voltage which is insufficient to cause data destruction even if the data read state is maintained during a period corresponding to a data refresh cycle required for refreshing said memory cell array, and equal to or lower than a second voltage which causes data destruction during a read operation.

3. The semiconductor memory device according to claim 2, wherein

said drain voltage of said selected memory cell is set in a voltage region in which a read time necessary for reading data of said selected memory cell to store in said data latch is not longer than a time length that induces cell data destruction by continuing the data read state.

4. The semiconductor memory device according to claim 1, wherein

a time of a write back operation performed by said sense amplifier circuit for said selected memory cell is shorter than that of an ordinary write operation.

5. The semiconductor memory device according to claim 1, wherein

a time of a write back operation performed by said sense amplifier circuit for said selected memory cell is shorter than that in a data refresh cycle.

6. The semiconductor memory device according to claim 1, further comprising:

a first transfer circuit configured to transfer the read data in said data latch of said sense amplifier to said output circuit; and

a second transfer circuit configured to write back the read data in said data latch into said selected memory cell, said second transfer circuit becoming on simultaneously with said first transfer circuit.

7. The semiconductor memory device according to claim 6, wherein

said second transfer circuit configured to serve for transferring data held in said data latch to said memory cell array in an ordinary write operation and a data refresh operation.

8. The semiconductor memory device according to claim 7, wherein

an on-state period of said second transfer circuit at when the write back is done into said selected memory cell is shorter than that at when said ordinary write operation is done and when data refresh operation is done.

9. The semiconductor memory device according to claim 1, wherein

said sense amplifier circuit further comprises a write back circuit configured to write back data into said selected memory cell only when the read data in said data latch is one in binary data which is disturbed during data read.

10. The semiconductor memory device according to claim 9, wherein

said write back circuit comprises first and second transistors serially connected between a transfer line for transferring write data to said memory cell array and a write back-use power supply line, said first transistor being gate-controlled by one data node of said data latch, said second transistor being gate-controlled by a control signal for writing back.

11. The semiconductor memory device according to claim 1, wherein

said sense amplifier circuit comprises:

an operational amp having a sense node to which a cell data is transferred and a reference node to which a reference voltage is applied;

said data latch connected to an output node of said operational amp for holding read data;

a first current source load connected to said sense node; and

a reference voltage generation circuit configured to have a second current source load connected to said reference node, and generate said reference voltage.

12. The semiconductor memory device according to claim 11, wherein

said reference voltage generation circuit comprises:

first and second reference cells connected to first and

second reference bit lines, respectively, into which different reference data are written; and

a switch circuit having first and second transfer gates for commonly connecting said first and second reference bit lines to said reference node during a data read operation, and third and fourth transfer gates for supplying different write-use voltages to said reference bit lines during a data write operation, respectively, and wherein

said second current source load has two times as high drivability as that of said first current source load.

13. The semiconductor memory device according to claim 12, wherein

reference data are written into said first and second reference cells simultaneously with the write back done into said selected memory cell.

14. The semiconductor memory device according to claim 12, further comprising:

first and second power supply lines connected to said first and second reference bit lines through said third and fourth transfer gates to which different reference data write-use voltages are applied, respectively.

15. The semiconductor memory device according to claim 12, further comprising:

first and second data lines connected to said first and second reference bit lines through said third and fourth transfer gates for writing reference data into said first and second reference cells, respectively.

16. The semiconductor memory device according to claim 1, wherein

said sense amplifier further comprises a clamp circuit for clamping a bit line of said memory cell array which is connected to said sense node during a data read operation, and

wherein

said reference voltage generation circuit further comprises a dummy clamp circuit for clamping said reference bit lines which are connected to said reference node during said data read operation.